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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/653,925	KELKAR ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,15-17,19-22,25,26 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,15-17,19-22,25,26 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 6, 21, 22, 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US Pat. 5691041) in view of Card, Jr. et al., (US Pat. 5300402), Ohshima et al. (US Pat. 5936843) and Love (US Pat. 5477160).

Regarding claim 1, Frankeny et al. disclose an integrated circuit (IC) package comprising:

- an IC die (1 in Fig. 6) having a top side and bottom side opposite to the top side, the top side of the die including raised interconnects/bumps (2 in Fig. 6) located over and conductively coupled to the die
- a solid flexible dielectric circuit film (FDCF)/interposer (see 3 in Fig. 6; Col. 2, line 30; Col. 5, line 30) having top and bottom surfaces, the FDCF being made of a single layer or a plurality of layers (Col. 4, line 61; Col. 5, line 30) the FDCF having outer landing pads/plated layer and inner landing pads/plated layer being formed on the top/bottom surfaces respectively (not numerically referenced- see pads at locations 11, 12, 13, etc. and over interconnects 2 in Fig. 6; also see

pads vias 6/7/8 in Fig. 2-4), the outer and inner landings/pads being fully supported by the circuit film, the outer and inner landings having a configuration such that the outer landing is being laterally offset from the inner landing (not numerically referenced- see outer pad at location 13 being connected to the inner pad under interconnect 2 in Fig. 6) or in alignment with the inner landing (not numerically referenced- see outer pad at location 11, 14, 18, etc. being connected to the inner pad under respective interconnects 2 in Fig. 6)

- the outer and inner landings being connected within the solid FDCF via a plated through-hole conductor (not numerically referenced- see the plated through-hole in Fig. 6; Col. 4, line 29)
- a routing conductor/internal wiring layer (16 in Fig. 6) extending laterally within the solid FDCF to provide the desired ground or power/signal connections (Col. 4, line 63)
- the FDCF being located over and conductively attached to the raised interconnects/bumps such that an air gap is formed between the IC die and the FDCF, the height of the air gap being less than the diameter of solder balls (see Fig. 6), and
- contact bumps/balls (9 in Fig. 6) being conductively coupled with the respective outer landings of the FDCF

(Fig. 6; Col. 4, line 30- Col. 6, line 65; Fig. 2-4).

Frankeny et al. fail to teach:

a) using at least one bond pad coupling the raised interconnect/bump on the topside of the die

b) the outer and inner landings being connected within the solid FDCF via a routing conductor extending laterally within the solid FDCF, and

c) the FDCF having a thickness of 10,000- 200,000 angstroms.

a) Ohshima et al. teach using an IC package where conventional bond pads couple the raised interconnect/bumps on a chip/die (74-1 and 82b respectively in Fig. 4; Col. 6, lines 10-50).

b) Love teaches using a thin film dielectric substrate (TFDS) in a single layer solid form (see 103 in Fig. 1a; Col. 4, lines 19-35) or a multilayered structure, if required for specific applications (Col. 4, line 37), the TFDS including an interconnection path/ routing conductor (see 110 and 112 within 103 in Fig. 1a) extending vertically and laterally within the single layer of the TFDS to provide the desired routing including offset connections between outer and inner landings (see offset connections between 107 and 106 respectively in Fig. 1a) on top and bottom surfaces respectively and to improve test/repair operations (Col. 4, line 54- Col. 5, line 11).

c) Frankeny et al. further teach the FDCF/interposer being formed of a variety of polymer coatings/formulations/films for different applications (Col. 5, lines 26-40), such polymer having a thickness as low as 0.5 mils or 125,000 angstroms as taught by Card, Jr. et al. (see Card, Jr. et al.: Col. 2, line 49; Col. 5, line 35; Col. 2-8).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the elements a)-c) as taught by Card, Jr. et al., Ohshima et al. and Love so that the desired package flexibility, offset between the bonding pad on the top and bottom surfaces of the substrate, the improved test/repair capability and the routing/interconnection can be achieved in Frankeny et al's package.

Regarding claim 2, Frankeny et al., Card, Jr. et al., Ohshima et al. and Love teach substantially the entire claimed structure as applied to claim 1 above, except the air gap being in a range of 10-500 microns.

Frankeny et al. further teach conventional solder balls having diameter of about 125 microns (Col. 2, line 15) providing the height the air gap being in a range of 10-500 microns.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the air gap/height being in a range of 10-500 microns so that the overall package size can be reduced and the test repair/inspection can be improved in Card, Jr. et al., Love, Ohshima et al. and Frankeny et al's package.

Regarding claim 5, Frankeny et al., Card, Jr. et al., Ohshima et al. and Love teach substantially the entire claimed structure as applied to claim 1 above, except a horizontal offset distance between the outer and inner landings being in a range of 50-1000 microns.

Frankeny et al. further teach using the spacing of conventional solder balls connected on the lands being 250 microns (Col. 2, line 15) such that the horizontal offset distance between the inner and outer landings falls in a range of 50-1000 microns.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the horizontal offset distance between the outer and inner landings being in a range of 50-1000 microns so that the desired terminal pitch/density conversion between the top and bottom surfaces of the substrate and the miniaturization of the IC can be achieved in Card, Jr. et al., Ohshima et al., Love and Frankeny et al's package.

Regarding claim 6, Frankeny et al., Card, Jr. et al., Ohshima et al. and Love teach substantially the entire claimed structure as applied to claim 1 above, wherein Frankeny et al. teach the contact bumps (9 in Fig. 6) being conductively coupled with the respective outer landings of the FDCF.

Regarding claim 21, Frankeny et al., Card, Jr. et al., Ohshima et al. and Love teach substantially the entire claimed structure as applied to claim 1 above, wherein Frankeny et al. teach the FDCF being made of multiple layers (Col. 5, line 30).

Regarding claim 22, Frankeny et al., Card, Jr. et al., Ohshima et al. and Love teach substantially the entire claimed structure as applied to claim 1 above, wherein Frankeny et al. teach connecting the outer and inner landings via a routing connector such as a plated through hole (not numerically referenced- see plated through hole connector connecting 2 and 9 at locations on top/bottom surfaces of 3 in Fig. 6; Col. 4, line 42) in such a way as to form a cantilever-like structure.

Regarding claims 29-31, Frankeny et al., Card, Jr. et al., Ohshima et al. and Love teach substantially the entire claimed structure as applied to claim 1 above, except the laterally extended segment of the routing conductor is necessarily required to connect the two landings and the routing conductor is formed into a step-like shape and two vertical segments are laterally offset and are necessarily connected together with the laterally extended segment.

Love further teaches the outer and inner bond pads/landings being connected within the TFDS via a step-shaped routing conductor extending vertically and laterally (see the shape of 110 in Fig. 1a) within the TFDS where the laterally extended segment (see the horizontal segment of 110 in Fig. 1a) is required/configured to provide the

desired connection between the two vertical segments and an offset between the inner and outer bond pads/landings. Furthermore, the lateral segment connects a first/top and second/bottom vertical segments (see two vertical segments of 110 in Fig. 1a), which further connect to the outer and inner landings/bonding pads at the top and bottom surfaces of the TFDS respectively.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the laterally extended segment of the routing conductor being necessarily required to connect the two landings, the routing conductor having a step-like shape, as taught by Love so that the desired routing and the offset between the top and bottom surfaces of the substrate can be achieved in Card, Jr. et al., Love, Ohshima et al. and Frankeny et al's package.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US Pat. 5691041), Card, Jr. et al. (US Pat. 5300402), Ohshima et al. (US Pat. 5936843) and Love (US Pat. 5477160) as applied to claim 1 above, and further in view of Wang et al. (US Pat. 6081026).

Regarding claim 3, Frankeny et al., Card, Jr. et al., Ohshima et al. and Love teach substantially the entire claimed structure as applied to claim 1 above, except the FDCF being substantially of the same size as the IC die.

Wang et al. teach using an IC package having a flexible dielectric circuit film (FDCF 100 in Fig. 1) where an IC die (104 in Fig. 1) has substantially the same size as the FDCF.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the FDCF being substantially of the same size as the IC die as taught by Wang et al. so that the package dimensions can be reduced and the fabrication/processing can be simplified in Card, Jr. et al., Love, Ohshima et al. and Frankeny et al's package.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US Pat. 5691041), Card, Jr. et al. (US Pat. 5300402), Ohshima et al. (US Pat. 5936843) and Love (US Pat. 5477160) as applied to claim 1 above, and further in view of Akagawa et al. (US Pat. 5834844).

Regarding claim 7, Frankeny et al., Card, Jr. et al., Love and Ohshima et al. teach substantially the entire claimed structure as applied to claim 1 above, except an under bump pad being formed over the bond pad and conductively coupling at least one bond pad and one raised interconnect.

Akagawa et al. teach using an IC (32 in Fig. 22) having a variety of conventional configurations of bonding pad/landings and an internal wiring where the under bump

pads (60 in Fig. 22) are formed over the bonding pad/landing portions and being conductively coupled to the raised interconnects/projection bumps (Fig. 22 and 26-28; Col. 8, line 26-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an under bump pad being formed over the bond pad and conductively coupling at least one bond pad and one raised interconnect.
as taught by Akagawa et al. so that the bond strength and interconnect reliability can be improved in Card, Jr. et al., Love, Ohshima et al. and Frankeny et al's package.

5. Claims 15, 16, 19, 20, 25, 26 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US Pat. 5691041) in view of Card, Jr. et al. (US Pat. 5300402), Ohshima et al. (US Pat. 5936843), Love (US Pat. 5477160) and Mizuno et al. (US Pat. 6077757).

Regarding claim 15, Frankeny et al. disclose an integrated circuit (IC) package comprising:

- an IC die (1 in Fig. 6) having a top side and bottom side opposite to the top side, the top side of the die including raised interconnects/bumps (2 in Fig. 6) located over and conductively coupled to the die
- a solid flexible dielectric circuit film (FDCF)/interposer (3 in Fig. 6; Col. 2, line 30; Col. 5, line 30) having top and bottom surfaces, the FDCF being made of a single

layer or a plurality of layers (Col. 4, line 61; Col. 5, line 30), the FDCF having outer landing pads/plated layer and inner landing pads/plated layer being formed on the top/bottom surfaces respectively (not numerically referenced- see pads at locations 11, 12, 13, etc. and over interconnects 2 in Fig. 6; also see pads vias 6/7/8 in Fig. 2-4), the outer and inner landings/pads being fully supported by the circuit film, the outer and inner landings having a configuration such that the outer landing is being laterally offset from the inner landing (not numerically referenced- see outer pad at location 13 being connected to the inner pad under interconnect 2 in Fig. 6) or in alignment with the inner landing (not numerically referenced- see outer pad at location 11, 14, 18, etc. being connected to the inner pad under respective interconnects 2 in Fig. 6)

- the outer and inner landings being connected within the solid FDCF via a plated through-hole conductor (not numerically referenced- see the plated through-hole in Fig. 6; Col. 4, line 29)
- a routing conductor/internal wiring layer (16 in Fig. 6) extending laterally within the solid FDCF to provide the desired ground or power/signal connections (Col. 4, line 63)
- the FDCF being located over and conductively attached to the raised interconnects/bumps such that an air gap is formed between the IC die and the
- FDCF, the height of the air gap being less than the diameter of solder balls (see Fig. 6), and

- contact bumps/balls (9 in Fig. 6) being conductively coupled with the respective outer landings of the FDCF

(Fig. 6; Col. 4, line 30- Col. 6, line 65; Fig. 2-4).

Frankeny et al. fail to teach:

a) at least one bond pad coupling the raised interconnect/bump on the topside of the die

b) the outer and inner landings being connected within the solid FDCF via a routing conductor extending laterally within the solid FDCF

c) the FDCF having a thickness of 10,000- 200,000 angstroms, and

d) the IC package having an IC wafer comprising a plurality of IC dice.

a) Ohshima et al. teach using an IC package where conventional bond pads couple the raised interconnect/bumps on a chip/die (74-1 and 82b respectively in Fig. 4; Col. 6, lines 10-50).

b) Love teaches using a thin film dielectric substrate (TFDS) in a single layer solid form (see 103 in Fig. 1a; Col. 4, lines 19-35) or a multilayered structure, if required for specific applications (Col. 4, line 37), the TFDS including an interconnection path/ routing conductor (see 110 and 112 within 103 in Fig. 1a) extending vertically and laterally within the single layer of the TFDS to provide the desired routing including

offset connections between outer and inner landings (see offset connections between 107 and 106 respectively in Fig. 1a) on top and bottom surfaces respectively and to improve test/repair operations (Col. 4, line 54- Col. 5, line 11).

c) Frankeny et al. further teach the FDCF/interposer being formed of a variety of polymer coatings/formulations/films for different applications (Col. 5, lines 26-40), such polymer having a thickness as low as 0.5 mils or 125,000 angstroms as taught by Card, Jr. et al. (see Card, Jr. et al.: Col. 2, line 49; Col. 5, line 35; Col. 2-8).

d) Mizuno et al. teach forming a conventional wafer scale package (WSP) package using a wafer and an insulating substrate (1 and 5 respectively in Fig. 4A-4F), the wafer comprising a plurality of IC die and being singulated to form a plurality of IC die packages (Col. 3, line 40- Col. 4, line 5, line 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the elements a) – d) above, as taught by Card, Jr. et al., Ohshima et al., Love and Mizuno et al. so that the desired routing, connection offset and cycle time can be achieved in Frankeny et al's IC package.

Regarding claim 16, Frankeny et al., Card, Jr. et al., Ohshima et al., Love and Mizuno et al. teach substantially the entire claimed structure as applied to claim 15 above, except the air gap being in a range of 10-500 microns.

Frankeny et al. further teach conventional solder balls having diameter of about 125 microns (Col. 2, line 15) providing the height the air gap being in a range of 10-500 microns.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the air gap/height being in a range of 10-500 microns so that the overall package size can be reduced and the test repair/inspection can be improved in Mizuno et al., Card, Jr. et al., Love, Ohshima et al. and Frankeny et al's package.

Regarding claim 19, Frankeny et al., Card, Jr. et al., Ohshima et al., Love and Mizuno et al. teach substantially the entire claimed structure as applied to claim 15 above, except a horizontal offset distance between the outer and inner landings being in a range of 50-1000 microns.

Frankeny et al. further teach using the spacing of conventional solder balls connected on the lands being 250 microns (Col. 2, line 15) such that the horizontal offset distance between the inner and outer landings falls in a range of 50-1000 microns.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the horizontal offset distance between the outer and inner landings being in a range of 50-1000 microns so that the desired terminal pitch/density conversion between the top and bottom surfaces of the substrate and the miniaturization of the IC can be achieved in Mizuno et al., Ohshima et al. and Frankeny et al's package.

Regarding claim 20, Frankeny et al., Card, Jr. et al., Ohshima et al. Love and Mizuno et al. teach substantially the entire claimed structure as applied to claim 15 above, wherein Frankeny et al. teach the contact bumps (9 in Fig. 6) being conductively coupled with the respective outer landings of the FDCF.

Regarding claim 25, Frankeny et al., Card, Jr. et al., Ohshima et al., Love and Mizuno et al. teach substantially the entire claimed structure as applied to claim 15 above, wherein Frankeny et al. teach the FDCF being made of multiple layers (Col. 5, line 30).

Regarding claim 26, Frankeny et al., Card, Jr. et al., Ohshima et al., Love and Mizuno et al. teach substantially the entire claimed structure as applied to claim 15 above, wherein Frankeny et al. teach connecting the outer and inner landings via a routing connector such as a plated through hole (not numerically referenced- see plated through hole

connector connecting 2 and 9 at location 13 2 in Fig. 6; Col. 4, line 42) in such a way as to form a cantilever-like structure.

Regarding claims 32-34, Frankeny et al., Card, Jr. et al., Ohshima et al., Love and Mizuno et al. teach substantially the entire claimed structure as applied to claim 15 above, except the laterally extended segment of the routing conductor is necessarily required to connect the two landings and the routing conductor are formed into a step-like shape and two vertical segments are laterally offset and are necessarily connected together with the laterally extended segment.

Love further teaches the outer and inner landings being connected within the TFDS via a step-shaped routing conductor extending vertically and laterally (see the shape of 110 in Fig. 1a) within the TFDS where the laterally extended segment (see horizontal segment of 110 in Fig. 1a) is required/configured to provide the desired connection between the two vertical segments and an offset between the inner and outer landings. Furthermore, the lateral segment connects a first and second vertical segments (see two vertical segments of 110 in Fig. 1a), which further connect to the outer and inner landings/bonding pads at the top and bottom surfaces of the TFDS respectively.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the laterally extended segment of the routing conductor being necessarily required to connect the two landings, the routing conductor

having a step-like shape and two vertical segments are laterally offset and are necessarily connected together with the laterally extended segment as taught by Love so that the desired routing and the offset between the top and bottom surfaces of the substrate can be achieved in Mizuno et al., Card, Jr. et al., Ohshima et al., Love and Frankeny et al's package.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US Pat. 5691041), Card, Jr. et al. (US Pat. 5300402), Ohshima et al. (US Pat. 5936843), Love (US Pat. 5477160) and Mizuno et al. (US Pat. 6077757) as applied to claim 15 above, and further in view of Akagawa et al. (US Pat. 5834844).

Regarding claim 17, Frankeny et al., Card, Jr. et al., Ohshima et al., Love and Mizuno et al. teach substantially the entire claimed structure as applied to claim 1 above, except an under bump pad being formed over the bond pad and conductively coupling at least one bond pad and one raised interconnect.

Akagawa et al. teach using an IC (32 in Fig. 22) having a variety of conventional configurations of bonding pad/landings and an internal wiring where the under bump pads (60 in Fig. 22) are formed over the bonding pad/landing portions and being conductively coupled to the raised interconnects/projection bumps (Fig. 22 and 26-28; Col. 8, line 26-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an under bump pad being formed over the bond pad and conductively coupling at least one bond pad and one raised interconnect as taught by Akagawa et al. so that the bond strength and interconnect reliability can be improved in Mizuno et al., Card, Jr. et al., Love, Ohshima et al. and Frankeny et al's package.

Response to Arguments

7. Applicant's arguments with respect to claims 1-3, 5-7, 15-17, 19-22, 25, 26 and 29-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

08-11-04

NITIN PAREKH
PATENT EXAMINER
TECHNOLOGY CENTER 2800